DESCRIPTION

TheUC3842A-BW/43A-BW/44A-BW/45A-BW,UC3842M/43M/44M/45M are fixed frequency current mode PWM controller. They are specially designed for OFF−Line and DC to DC converter applications with a minimal external components. Internally implemented circuits include a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET. Protection circuitry includes built under voltage lockout and current limiting.

The UC3842A-BW, UC3844A-BW,UC3842M and UC3844M have UVLO thresholds of 16 V (on) and 10 V (off). The corresponding thresholds for the UC3843A-BW/45A-BW/43M/45M are 8.4V (on) and 7.6V (off). The UC3842A-BW, UC3843A-BW, UC3842M and UC3843M can operate within 100% duty cycle. The UC3844A-BW, UC3845A-BW, UC3844M and UC3845M can operate within 50% duty cycle.

The UC384XA-BW and UC384XM have Start-Up Current 0.17mA (typ).

The UC384XA-BW and UC384XM are revised UC384XAM and differ by higher Unity Gain bandwidth of Error Amplifier.

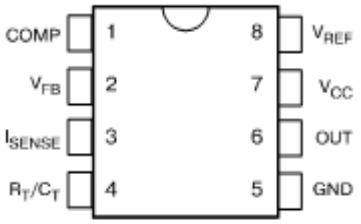
The UC3842ML/44ML are revised UC3842M/44M and differ by reduced Start-Up Current.

FEATURES

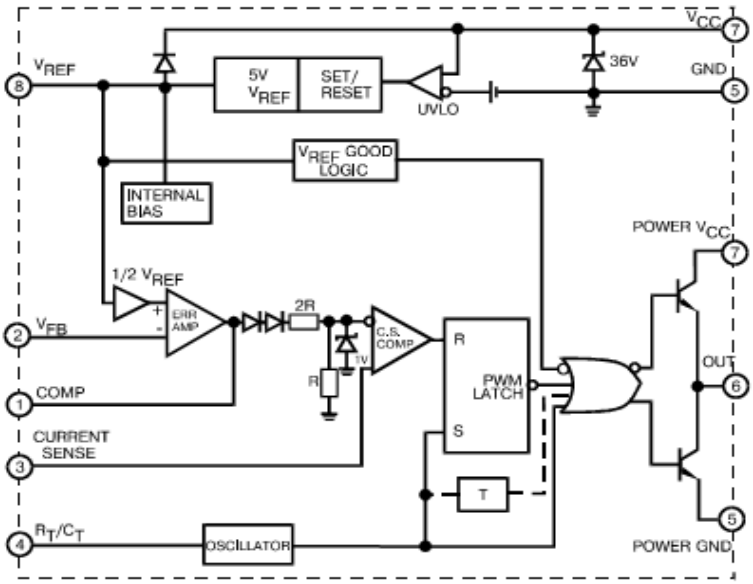
- Low Start-Up and Operating Current
- High Current Totem Pole Output
- Under voltage Lockout With Hysteresis
- Operating Frequency Up To 500KHz

PACKAGE INFORMATION

PIN CONNECTION
(TOP VIEW)



BLOCK DIAGRAM (toggle flip flop used only in UC3844, UC3845)



Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply Voltage (low impedance source)	VCC	30	V
Output Current	Io	±1	A
Input Voltage (Analog Inputs pins 2,3)	VI	−0.3 to 5.5	V
Error Amp Output Sink Current	I sink(E.A)	10	mA
Power Dissipation (TA=250C)	PO	1	W
Storage Temperature Range	Tstg	-65 to150	℃
Lead Temperature (soldering 5 sec.)	TL	260	℃

Electrical characteristics(*Vcc=15V,Rt=10kΩ, Ct=3.3nF, TA=0℃to+70℃, unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Section						
Reference Output Voltage	VREF	TJ = 25 ° C, IREF= 1 mA	4.9	5.0	5.1	V
Line Regulation	ΔVREF	12V ≤ Vcc≤ 25 V		6.0	20	mV
Load Regulation	ΔVREF	1 mA ≤IREF≤20mA		6.0	25	
Short Circuit Output Current	ISC	TA = 25 ° C		-100	-180	mA
Oscillator Section						
Oscillation Frequency	f	TJ= 25 ° C	47	52	57	KHz
Frequency Change with Voltage	Δf/ΔVCC	12V ≤Vcc≤ 25 V		0.05	1.0	%
Oscillator Amplitude	V(OSC)	(peak to peak)		1.6		V
Error Amplifier Section						
Input Bias Current	Ibias	VFB=3V		-0.1	-2	µA
Input Voltage	VI(E.A)	Vpin1= 2.5V	2.42	2.5	2.58	V
Open Loop Voltage Gain	Avol	2V ≤V0≤ 4V	65	90		dB
Unity Gain Bandwidth	UGBW	Tj=25℃, Note 3	0.5	0.6		MHz
Power Supply Rejection Ratio	PSRR	12V≤Vcc≤25 V	60	70		dB
Output Sink Current	ISINK	V pin2=2.7V, V pin1= 1.1V	2	7		mA
Output Source Current	ISOURCE	Vpin2= 2.3V, Vpin1= 5V	-0.5	-1.0		mA
High Output Voltage	VOH	Vpin2= 2.3V, RL= 15KΩto GND	5.0	6.0		V
Low Output Voltage	VOL	V= 15KΩto PIN 8		0.8	1.1	
Current Sense Section						
Gain	GV	(Note 1 & 2)	2.85	3.0	3.15	V/V
Maximum Input Signal	Vi(MAX)	Vpin1= 5V (Note1)	0.9	1.0	1.1	V
Supply Voltage Rejection	SVR	12V≤VCC≤25 V (Note 1)		70		dB
Input Bias Current	IBIAS	Vpin3 = 3V		-3.0	-10	µA
Output Section						

Low Output Voltage	VOL	ISINK= 20 mA		0.08	0.4	V
		ISINK= 200 mA		1.4	2.2	
High Output Voltage	Voh	ISINK= 20 mA	13	13.5		
		ISINK= 200 mA	12	13.0		
Rise Time	tR	TJ = 25 ° C, CL= 1nF (Note 3)		45	150	nS
Fall Time	tF	TJ= 25 ° C, CL= 1nF (Note 3)		35	150	
Undervoltage Lockout Section						
Start Theshold	VTH(ST)	UC3842A-BW/44A-BW/42M /44M	14.5	16.0	17.5	V
		UC3843A-BW/45A-BW/43M /45M	7.8	8.4	9.0	
Min. Operating Voltage (After Turn On)	VOPR(min)	UC3842A-BW/44A-BW/42M /44M	8.5	10	11.5	V
		UC3843A-BW/45A-BW/43M /45M	7.0	7.6	8.2	
PWM Section						
Max. Duty Cycle	D(MAX)	UC3842A-BW/43A-BW/42M /43M	95	97	100	%
		UC3844A-BW/45A-BW/44M /45M	47	48	50	
Min. Duty Cycle	D(MAX)				0	
Total Standby Current						
Start−Up Current	IST	UC3843A-BW,UC3845A-BW UC3843M, UC3845M		0.13	0.3	mA
		UC3842A-BW,UC3844A-BW UC3842M, UC3844M		0.2	0.3	
		UC3842ML, UC3844ML		0.17	0.25	
Operating Supply Current	ICC(OPR)	Vpin3= Vpin2= 0V		13	17	
Zener Voltage	VZ	Icc=25 mA	30	38		V

* Adjust Vcc above the start threshold before setting it to 15V.

Note 1: Parameter measured at trip point of latch with Vpin2=0.

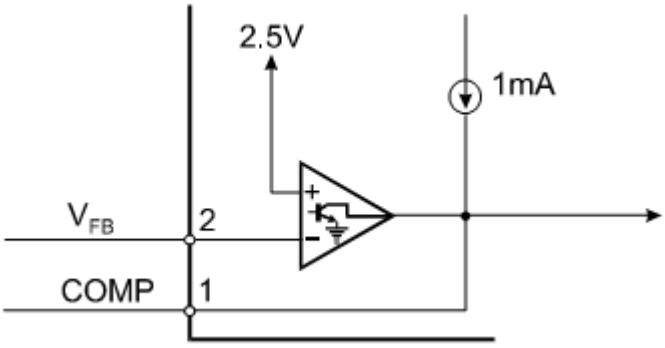
Note 2: Gain defined as A=ΔVpin1/ΔVpin3 ; 0 ≤ Vpin3 ≤ 0.8V.

Note 3: These parameters, although guaranteed, are not 100% tested in production.

Pin Assignment

N	FUNCTION	DESCRIPTION
1	COMP	This pin is the Error Amplifier output and is made for loop compensation.
2	VFB	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	ISENSE	voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	RT/CT	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor RT to Vref and capacitor CT to ground.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sink by this pin.
7	Vcc	This pin is the positive supply of the integrated circuit.
8	Vref	This is the reference output. It provides charging current for capacitor CT through resistor

APPLICATION INFORMATION



F gure 1. Error Amp Configuration

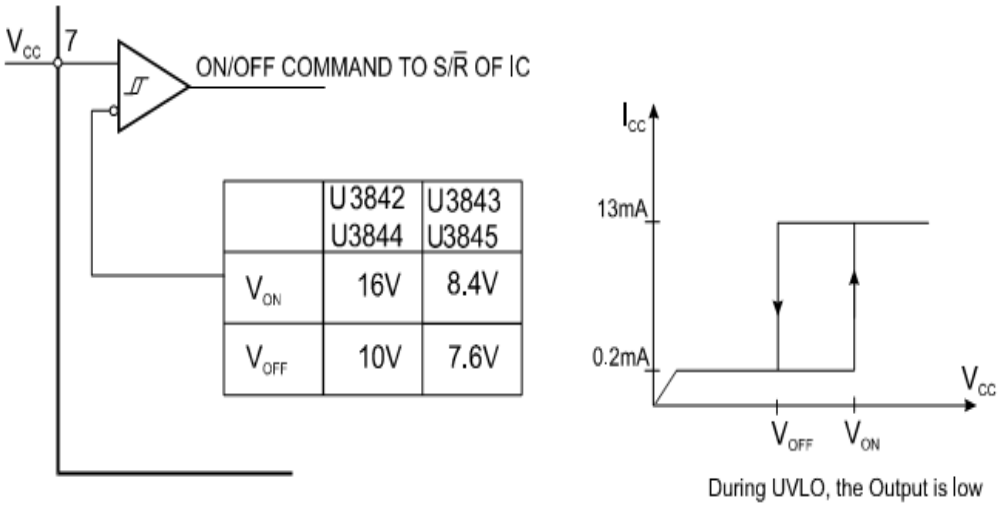


Figure 2. Under voltage Lockout

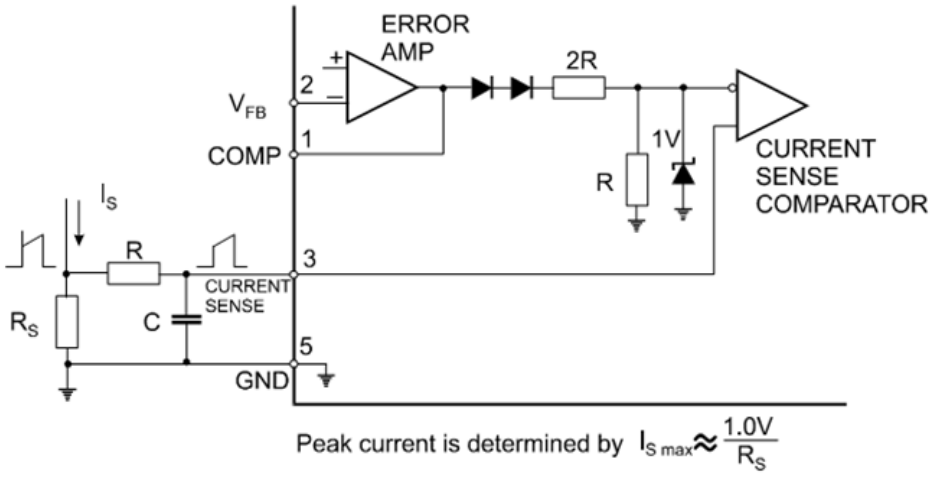


Figure 3. Current Sense Circuit

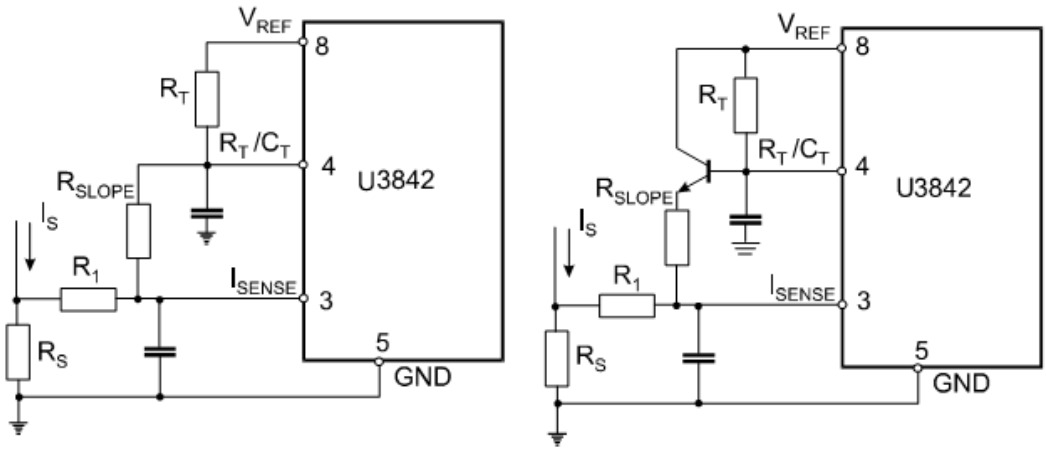


Figure 4. Slope Compensation Techniques

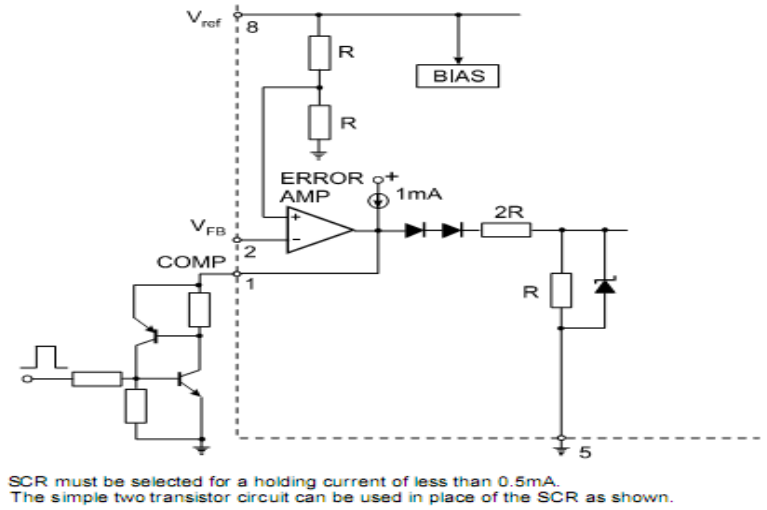
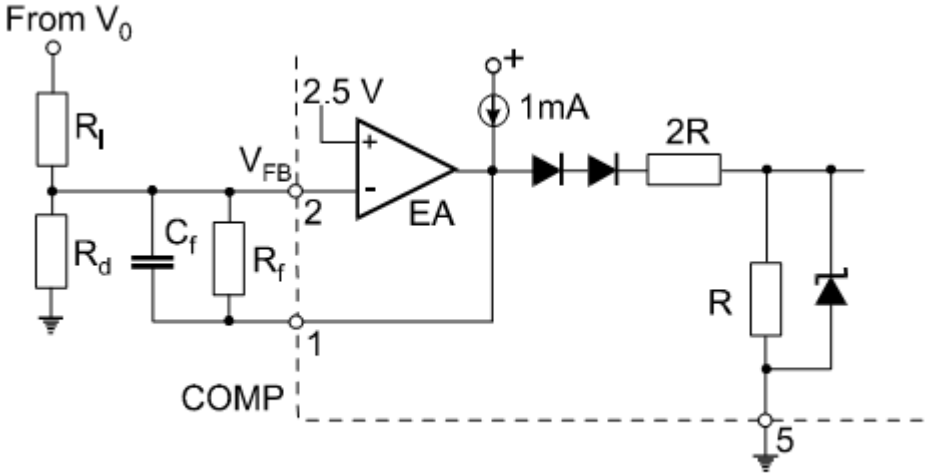
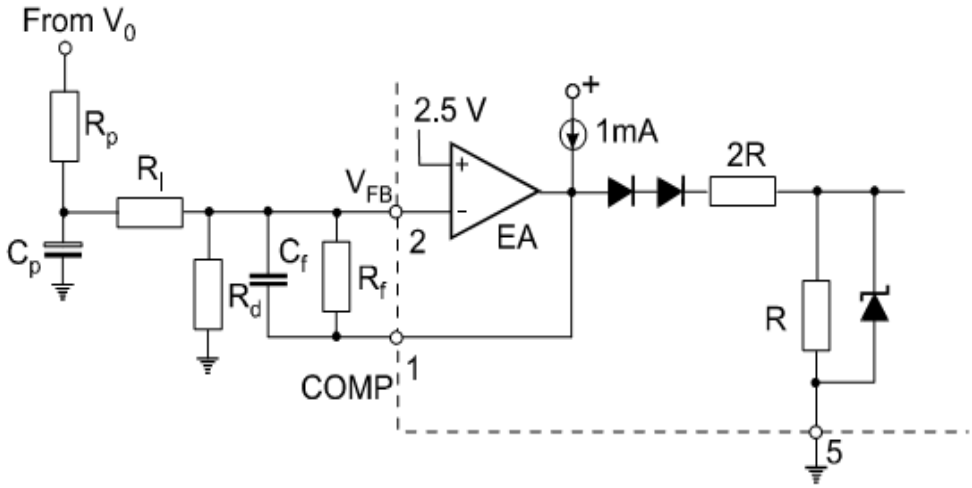


Figure 5. Latched Shutdown



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 6. Error Amplifier Compensation

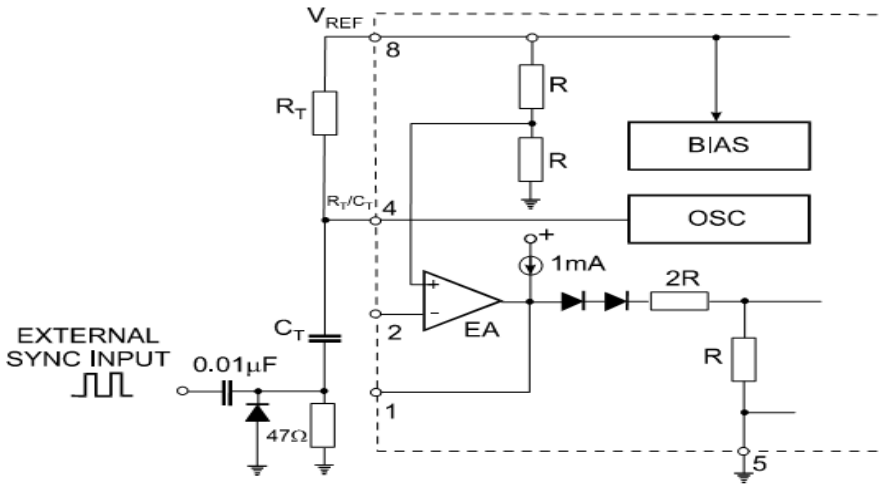


Figure 7. External Clock Synchronization

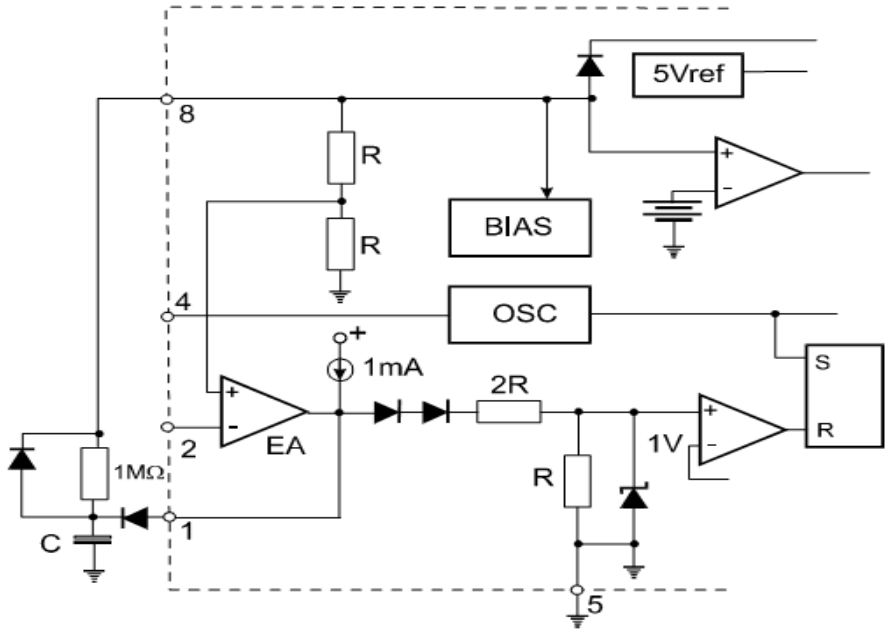


Figure 8. Soft-Start Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

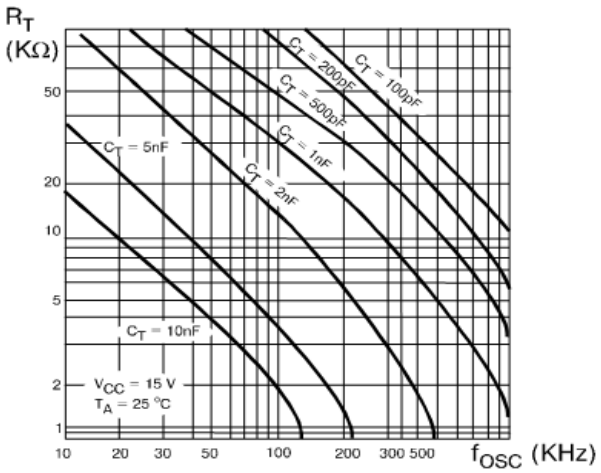


Figure 1. Timing Resistor vs. Oscillator Frequency

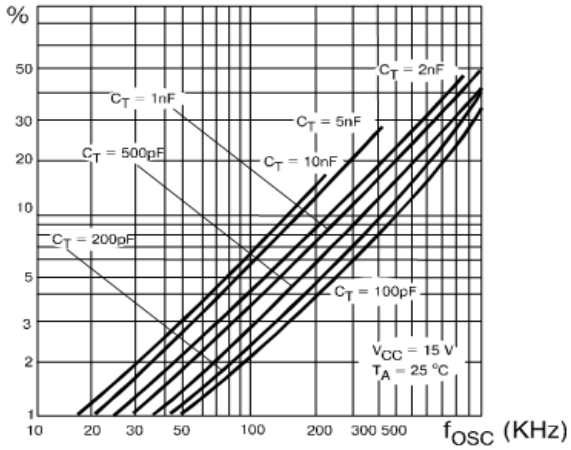


Figure 2. Output Dead-Time vs. Oscillator Frequency

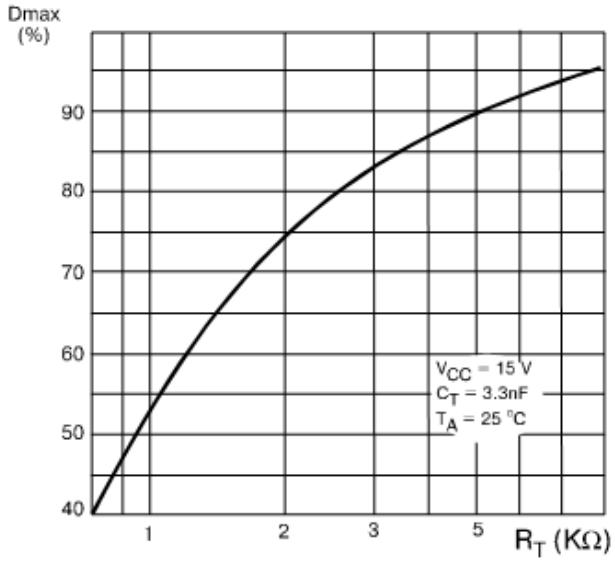


Figure 3. Maximum Output Duty Cy cle vs. Timing Resistor (U3842/43)

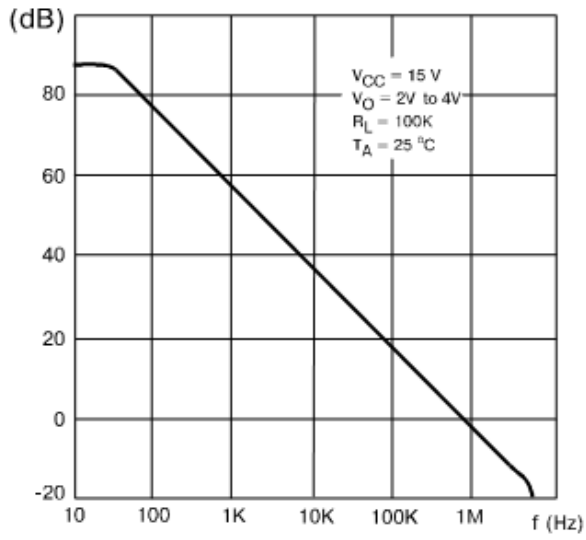


Figure 4. Error Amp Open-Loop Gain vs. Frequency

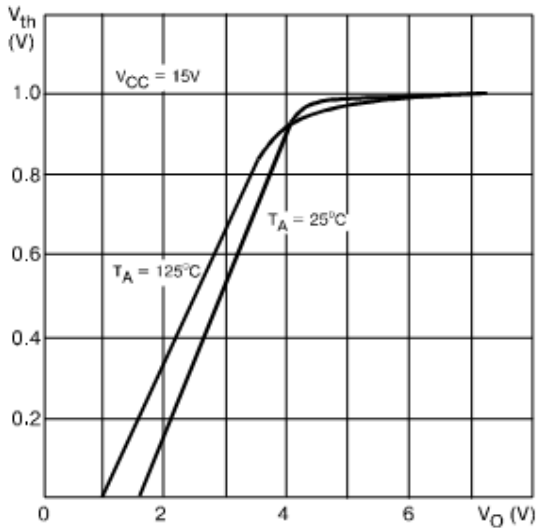


Figure 5. Current Sense Input Threshold vs. Error Amp Output Voltage

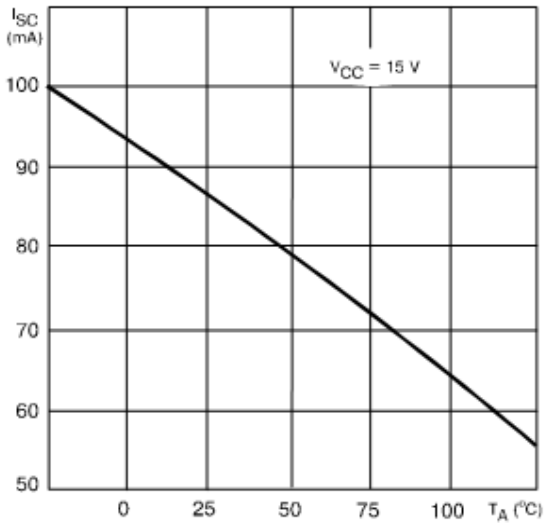


Figure 6. Reference Short Circuit Current vs. Temperature

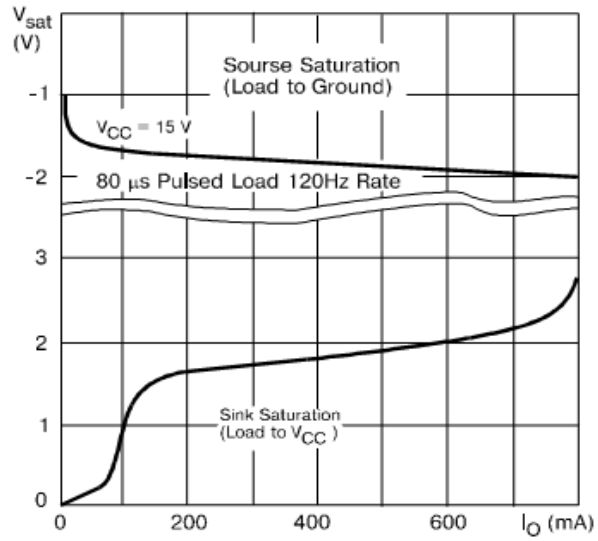


Figure 7. Output Saturation Voltage vs. Load Current
TA = 25 ° C

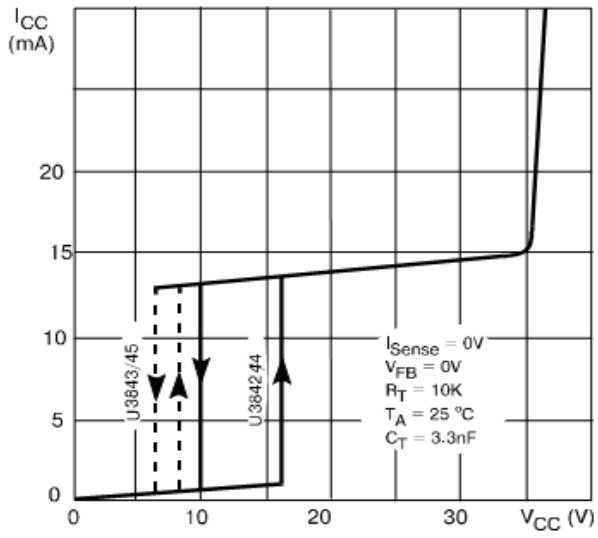


Figure 8. Supply Current vs. Supply Voltage

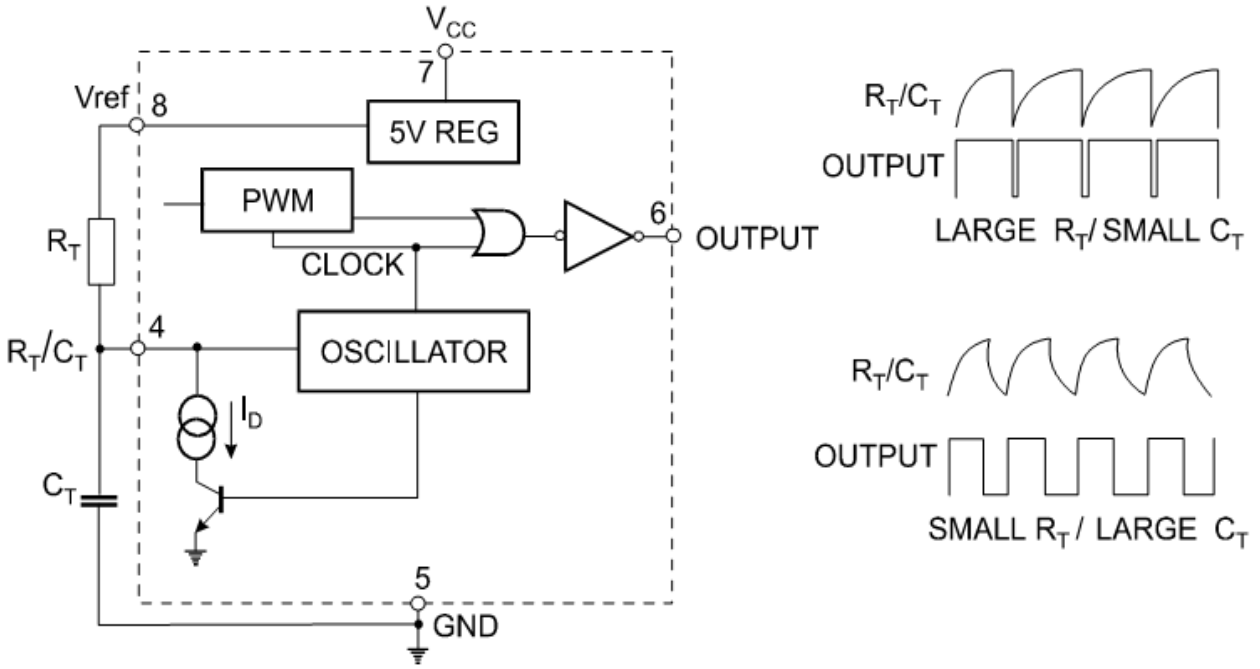
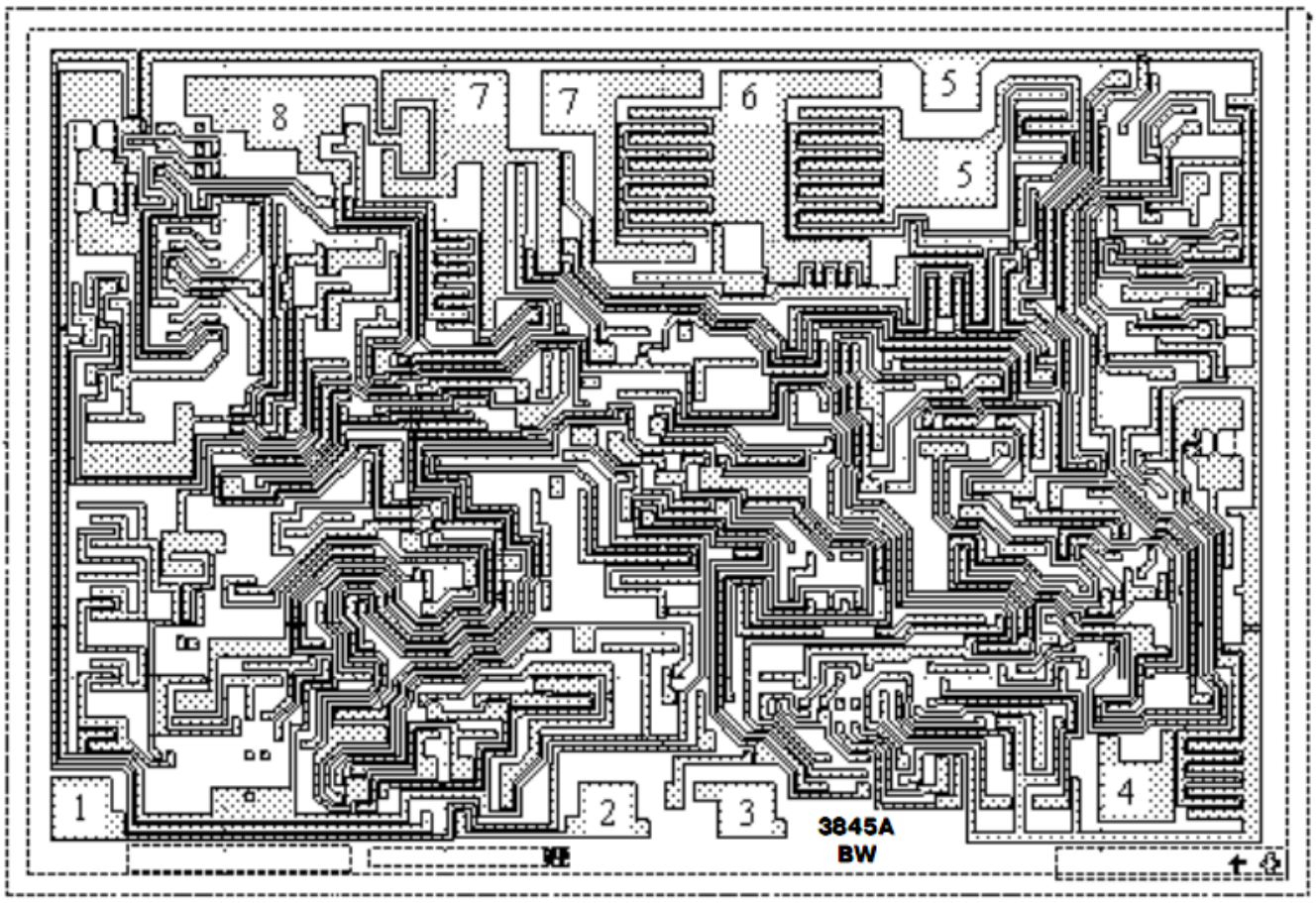


Figure 9. Oscillator and Output Waveforms

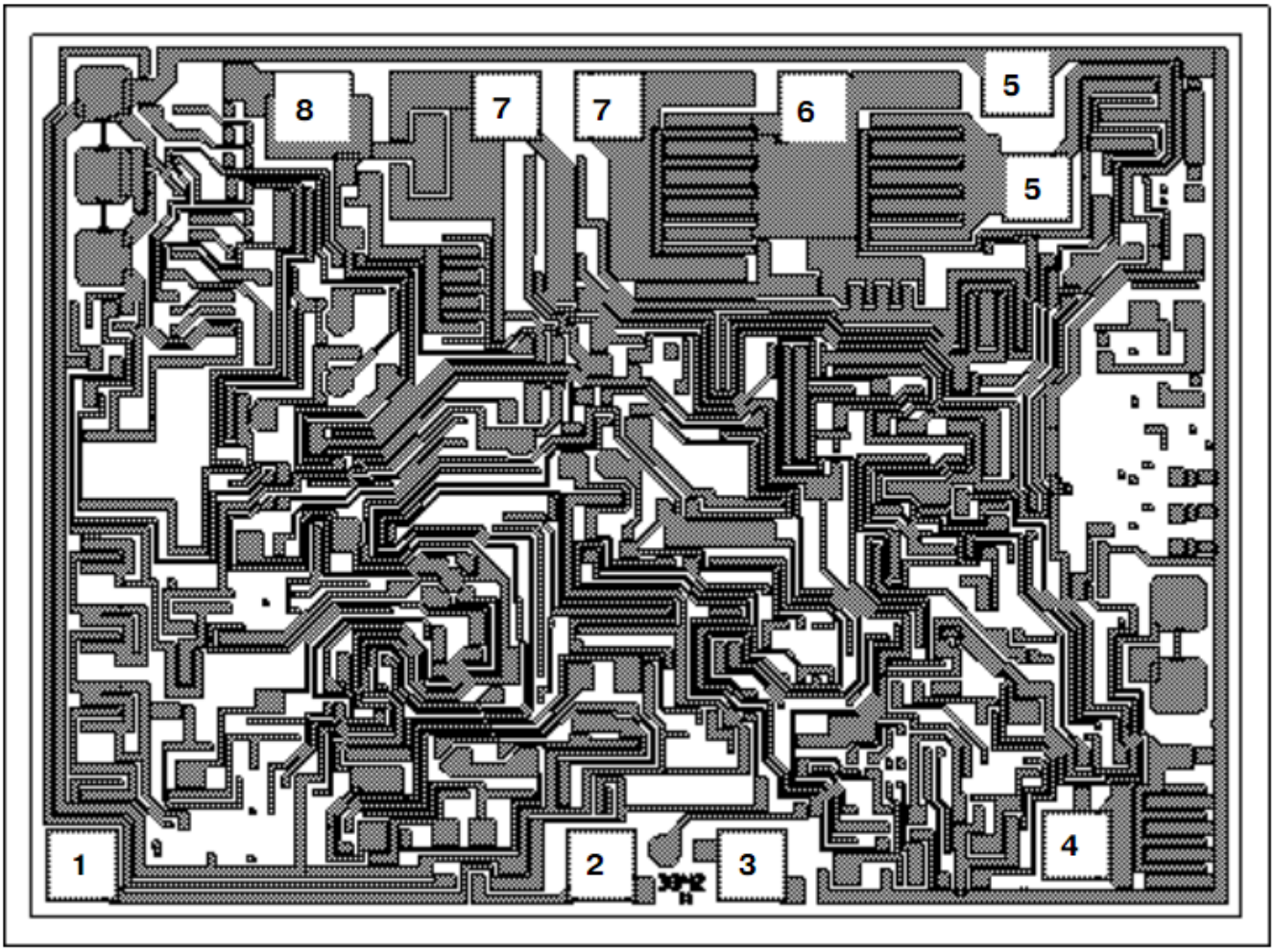
PAD LOCATION



Chip size: 2.38 x 1.63 mm ^{2}

PAD LOCATION COORDINATES

Pad N	Pad Name	Coordinates, μm	
		X	Y
1	COMP	90	110
2	VFB	1050	110
3	Isense	1310	110
4	RT/CT	2000	150
5	POWERGND	1700	1280
5	GND	1680	1450
6	OUT	1310	1410
7	POWERVcc	990	1410
7	VCC	815	1410
8	Vref	460	1390



Chip size: 1.82 x 1.35 mm ^{2}

Pad N	Pad Name	Coordinates, μm	
		X	Y
1	COMP	114	115
2	VFB	861	115
3	Isense	1077	115
4	RT/CT	1545	143
5	POWERGND	1487	1090
5	GND	1459	1240
6	OUT	1167	1207
7	POWERVcc	873	1207
7	VCC	723	1207
8	Vref	453	1207

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